AMENDMENTS TO THE DRAWINGS

Please replace Figures 1D, 1E, 2A, 2C, 3, 5, 7, 12, 13, 14 and 17, with the attached Replacement Sheets. Annotated marked-up drawings are also provided that identify the changes in the above noted Figures.

Remarks

Claims 1, 3-27 and 29-32 are presently pending in the subject application[1]. Claim 31 is allowed. Claims 3, 5, 6, 7, 10, 11, 14, 15, 18-24, 27, 29 and 30 have been objected to. Claims 1, 4, 7, 9, 12, 13, 16, 17, 25, 26 and 32 have been rejected.

Specification

The Amendments to the Specification were made to cure typographical errors and to improve the formatting of the application. Specifically, the polynomials expressed in the application were amended to place exponents into a superscript format. No new matter was introduced through these corrections.

Claims

The Amendments to the Claims section includes amendments to claims 5, 6, 11, 14, 15, 16, 20, 22 and 29 and addition of new claims 33-37. Claim 33 was added to re-introduce the subject matter originally claimed in the first claim 28 of the original application. Claims 34-37 were added to better claim that which the applicant believes is his invention. Claims 11, 16, 20, 22 and 29 were amended to better claim that which the applicant considers his invention. Claims 5, 6, 14 and 15 were amended to place polynomials recited therein in superscript format.

Support for new claim 33 is found in claim 28 as originally filed. Support for new claims 34-37 is found at least at page 14, line 20 through page 20, line 4 and at page 30, lines 4-29.

Claim Objections

Claim 16 has been objected to by the Examiner under 37 CFR 1.75(c) for failing to further limit the subject matter of the claim from which it depends. The applicant has amended claim 16 to recite further process over that recited in claim 13. With this change, the objection is traversed.

Claim Rejections – 35 U.S.C. 112

Claim 9 has been rejected by the Examiner under 35 U.S.C. §112, first paragraph for failing to comply with the written description requirement. Specifically, the Examiner has stated that the concept of "six pair combinations of column elements can be equated to a data row element pair" has not been disclosed. The applicant points out, however, that at least at page 13,

[1] The Examiner noted that the Preliminary Amendment filed 18 January 2005 was not entered. The Examiner has, however, canceled claims 2 and both claims 28 as a result of the Preliminary Amendment. Accordingly, the applicant has treated the claims in the present amendment as not having been modified from the claims as originally filed except for the cancellation of claims 2 and both claims 28.

lines 18 – 20 the specification teaches that "[w]ith ts = the data byte and vu = the ECC byte and st, su, sv, tu, tv, and uv, are row couplets mirroring the data byte [Di] = st and wx, wy, wz, xy, xz and yz are column couplets also mirroring the data byte [Di] = st." (Emphasis added). This is ample support for claim 9 and the rejection is therefore traversed.

Claim Rejections – 35 U.S.C. 102(b)

Claims 1, 4 and 12 stand rejected under 35 U.S.C. 102(b) as anticipated by U.S. Patent 6,158, 026 ("Kawahara"). The applicant has carefully studied Kawahara and believes that these claims in their present form define subject matter not taught or suggested by Kawahara.

The presently rejected claims are directed to a method for encoding a data byte for use in computer, communication and storage systems. Specifically the method includes the steps of selecting an irreducible polynomial, generating an error control code (ECC) from the polynomial and the data to be encoded, generating an encoded data matrix where elements of the matrix are based on the ECC and distributing the elements to one of multiple channels where the channel selected for a particular element is dependent upon the position of the element in the matrix.

The Examiner cites Kawahara as teaching all of the elements. In particular, the Examiner cites Kawahara at Fig. 4, elements 35-50 (recording heads) as teaching dispersing an element of the encoded data matrix to a selected one of a plurality of channels base upon a position of the element in the matrix. Kawahara teaches a method for translating data to a data form that is more reliably recorded and recovered due to the data frequency of ones and zero. Kawahara serial recording system does not, however, disperse data or introduce data redundancy into the data being recorded.

In reviewing the text supporting Fig. 4 (primarily column 7, line 20 through column 8, line 60), the applicant has found the specification silent on the point of dispersing an element to a location based on its position in the matrix. To begin with, heads 43-50 are playback heads of a recorder and it is clear that none of the data produced by the Kawahara recorder is sent to these heads. In fact, Kawahara determines which head will receive audio and video data through use of a servo 58 (see column 7, lines 59-63). Because Kawahara does not teach all of the elements present in claim 1, the rejection of claim 1 is traversed. Because claim 1 is presently in allowable form, claims 4 and 12 that depend from claim 1 are allowable as well.

Further, with respect to claim 4, the Examiner cites Kawahara as teaching the use of an eighth order polynomial (see column 2, line 35). The applicant notes that the polynomial

referenced by the Examiner is used for generation of an M sequence to scramble data, not to generate an error correction code as presently claimed. Because Kawahara does not teach the use of the eighth order polynomial as presently claimed, the rejection of claim 4 is traversed for this additional reason.

Claim Rejections – 35 U.S.C. 103(a)

Claims 7, 12, 13, 16, 17, 25 and 26 have been rejected under 35 U.S.C. 103(a) as being obvious from Kawahara in view of U.S. Patent 4,513,420 ("Collins"). Collins is cited by the Examiner as teaching generation of an ECC through division of data by a polynomial.

Claim 13 specifically claims formation of an error correction code being in the form of d0d1d2d3d4d5d6d7e0e1e2e3e4e5e6e7. After careful review of the Collins reference no teaching or suggestion of such a code form was found or suggested. Indeed, Collins is silent on the structure of the error correction code. Accordingly, because the combination of references still does not teach or suggest all of the elements of the present claims, the rejection is traversed.

Claims 25 and 26 recite further steps to claim 13 for encoding data. Claim 25 adds the concept of arranging the matrix so that each element of the data byte is horizontally or vertically adjacent to at least three other elements of the data byte. Claim 26 claims the step of making arranging the matrix so that each element of the data byte and the error control byte is a row of the matrix. As noted above, Collins is silent on the structure of the error correction code and the matrix produced thereby. Accordingly, because the combination of references still does not teach or suggest all of the elements of the present claim. The rejection is traversed. Further, because claims 25 and 26 depend from allowable claim 13, claims 25 and 26 are allowable as well.

For at least the reason that claims 7 and 12 are dependent upon allowable claim 1, claims 7 and 12 are allowable as well. For at least the reason that claims 16 and 17 are dependent upon allowable claim 13, claims 16 and 17 are allowable as well.

Drawing

In the drawings, a number of replacement sheets are submitted to correct typographical errors or to enhance the readability of the figures. All of the drawing figure changes, with the exception of Figure 1E and 3, have been amended to look as they did in United States Provisional Patent Application Nos. 60/399,635 entitled "Data Dispersion and Mirroring Method

with Fast Dual Erasure Correction and Multi-Dimensional Capabilities" filed on July 29, 2002, and 60/460,545 entitled "Composite Data Protection Method for Micro Level Data" filed April 4, 2003. Since these applications were incorporated into the present application by reference, no new matter has been added through these changes.

With respect to Figure 1E, the changes are supported by at least the text in paragraphs 0077 through 0080.

With respect to Figure 3, the changes are supported by at least the text in paragraph 0062.

The Figures submitted with the Preliminary Amendment were not identified as "Replacement Sheets." The applicant has so identified the Figures submitted with this Amendment.

If any fee is required for entry of this paper, the Commissioner is authorized to charge Deposit Account No. 06-0029 and is requested to notify us of the same.

Respectfully Submitted,

ROBERT HALFORD

Date: April 17, 2005

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Customer No. 25764

M2:20789300.02

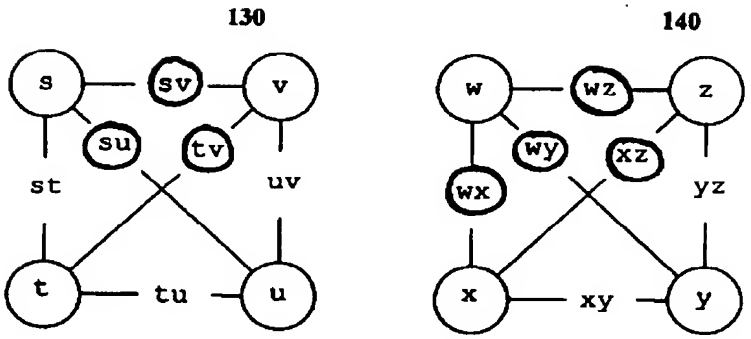

130
140
s
sv
v
su
tv
st
uv
t
tu
u
w
wz
z
wy
xz
wx
yz
x
xy
y

FIG 1D

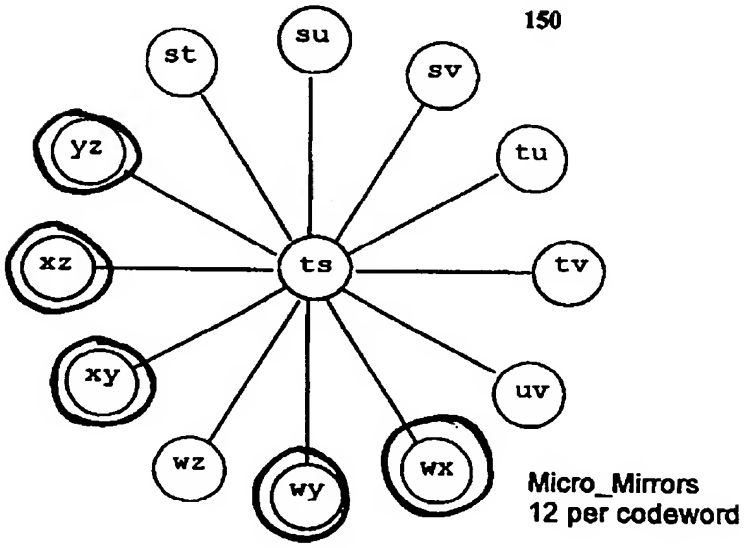

150
su
st
sv
yz
tu
xz
ts
tv
xy
uv
wz
wy
wx
Micro_Mirrors
12 per codeword

FIG 1E

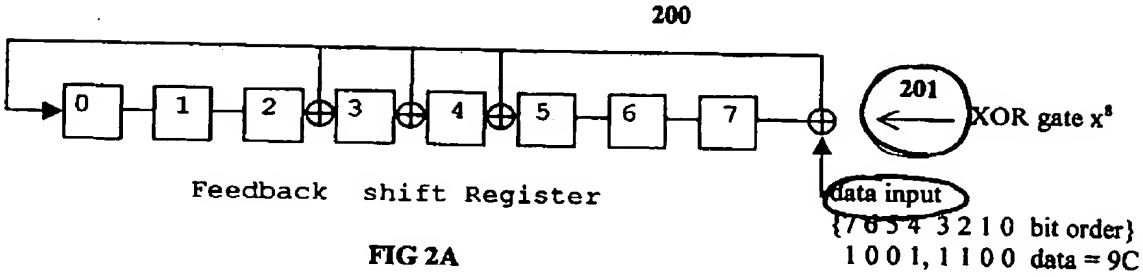


FIG 2A

0	0	0	0	0	0	0	0	
1	0	0	1	1	1	0	0	results after 1 shift
0	1	0	0	1	1	1	0	results after 2 shifts
0	0	1	0	0	1	1	1	results after 3 shifts
0	0	0	1	0	0	1	1	results after 4 shifts
0	0	0	0	1	0	0	1	results after 5 shifts
0	0	0	0	0	1	0	0	results after 6 shifts
0	0	0	0	0	0	1	0	results after 7 shifts
0	0	0	0	0	0	0	1	results after 8 shifts, ECC = 80

FIG 2B

210

e0 = d0 + d3 + d4 + d5 + d6
e1 = d1 + d4 + d5 + d6 + d7
e2 = d2 + d5 + d6 + d7
e3 = d0 + d4 + d5 + d7
e4 = d0 + d1 + d3 + d4
e5 = d0 + d1 + d2 + d3 + d6
e6 = d1 + d2 + d3 + d4 + d7
e7 = d2 + d3 + d4 + d5

per example

0 + 1 + 1 + 0 + 0 = 0
0 + 1 + 0 + 0 + 1 = 0
1 + 0 + 0 + 1 = 0
0 + 1 + 0 + 1 = 0
0 + 0 + 1 + 1 = 0
0 + 0 + 1 + 1 + 0 = 0
0 + 1 + 1 + 1 + 1 = 0
1 + 1 + 1 + 0 = 1

ECC = 80 for data byte 9C

FIG 2C

220

d0 = e2 + e3 + e4 + e5
d1 = e0+ e3 + e4 + e5 + e6
d2 = e1 + e4 + e5 + e6 + e7
d3 = e3 + e4 + e6 + e7
d4 = e0 + e2 + e3 + e7
d5 = e0 + e1 + e2 + e5
d6 = e0 + e1 + e2 + e3 + e6
d7 = e1 + e2 + e3 + e4 + e7

per example

0 + 0 + 0 + 0 = 0
0 + 0 + 0 + 0 + 0 = 0
0 + 0 + 0 + 0 + 1 = 1
0 + 0 + 0 + 1 = 1
0 + 0 + 0 + 1 = 1
0 + 0 + 0 + 0 = 0
0 + 0 + 0 + 0 + 0 = 0
0 + 0 + 0 + 0 + 1 = 1

data byte = 9C for ECC = 80

FIG 2D

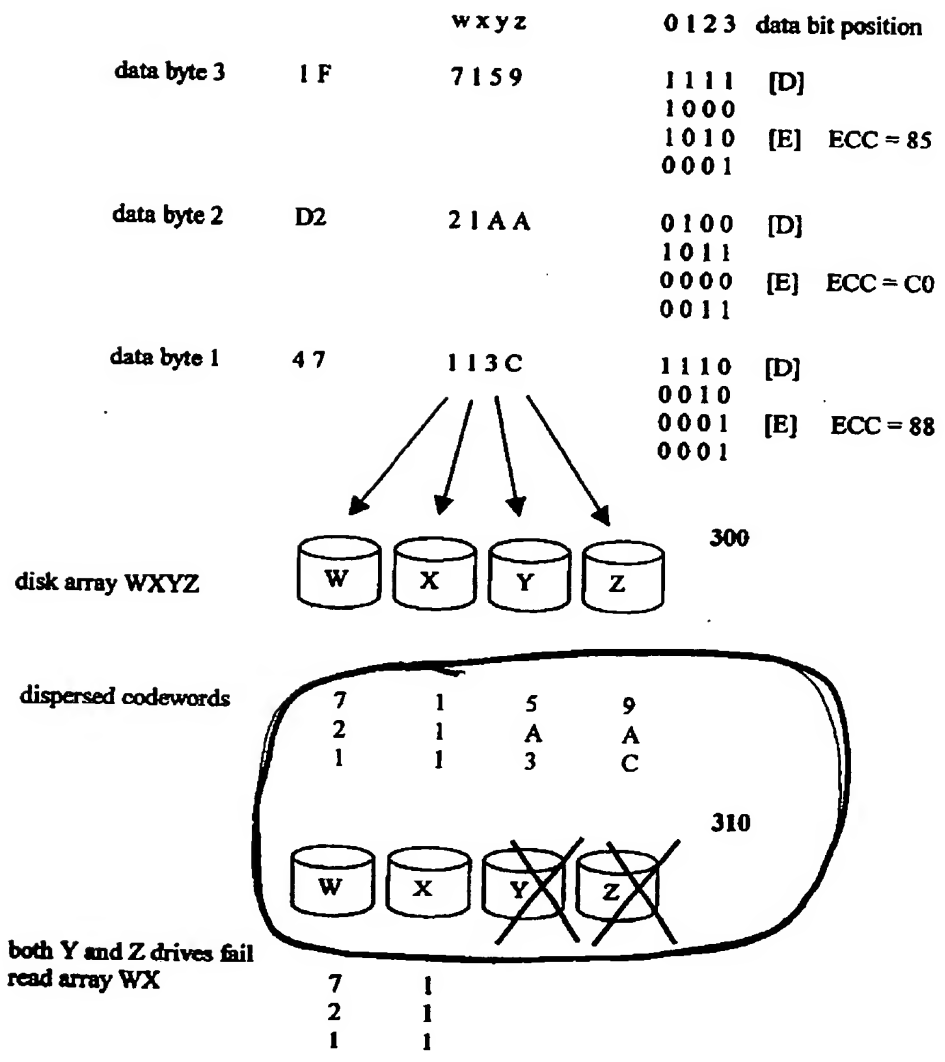

w x y z
0 1 2 3 data bit position
data byte 3
1 F
7 1 5 9
1 1 1 1 [D]
1 0 0 0
1 0 1 0 [E] ECC = 85
0 0 0 1
data byte 2
D2
2 1 A A
0 1 0 0 [D]
1 0 1 1
0 0 0 0 [E] ECC = C0
0 0 1 1
data byte 1
4 7
1 1 3 C
1 1 1 0 [D]
0 0 1 0
0 0 0 1 [E] ECC = 88
0 0 0 1
300
disk array WXYZ
W
X
Y
Z
dispersed codewords
7 1 5 9
2 1 A A
1 1 3 C
310
W
X
Y
Z
both Y and Z drives fail
read array WX
7 1
2 1
1 1
Recovered Data
1F
D2
47

FIG 3

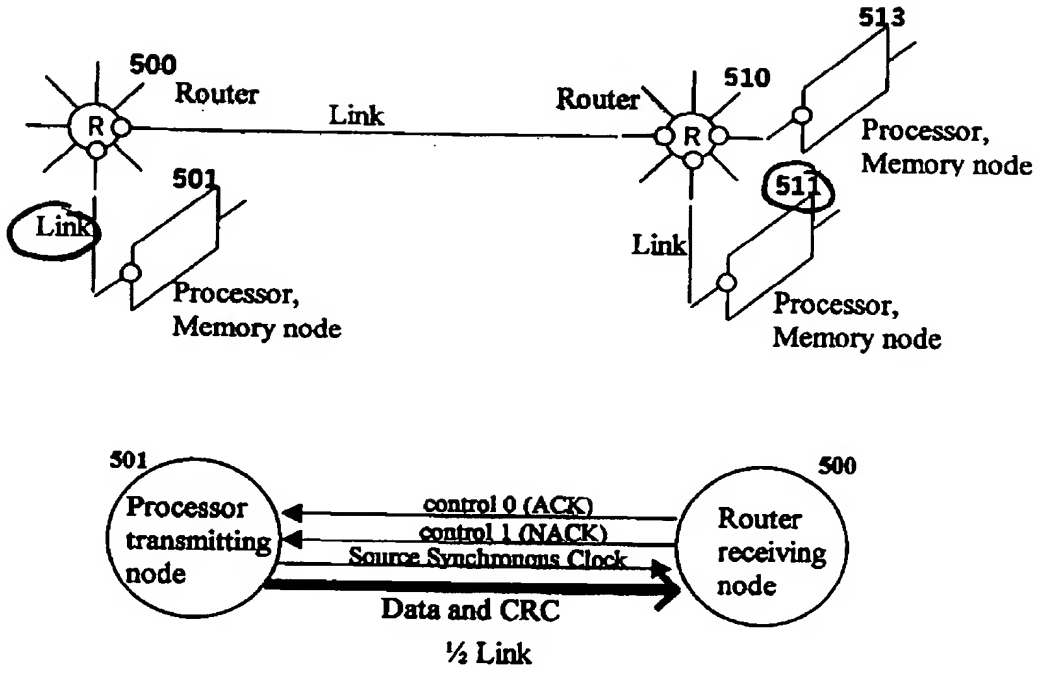


FIG 5

600

byte	8	7	6	5	4	3	2	1	0
	c	d	d	d	d	d	d	d	d
	c	d	d	d	d	d	d	d	d
	c	d	d	d	d	d	d	d	d
	c	d	d	d	d	d	d	d	d
	c	d	d	d	d	d	d	d	d
	c	d	d	d	d	d	d	d	d
	c	d	d	d	d	d	d	d	d
	c	d	d	d	d	d	d	d	d

Data Flow >>>>

FIG 6A

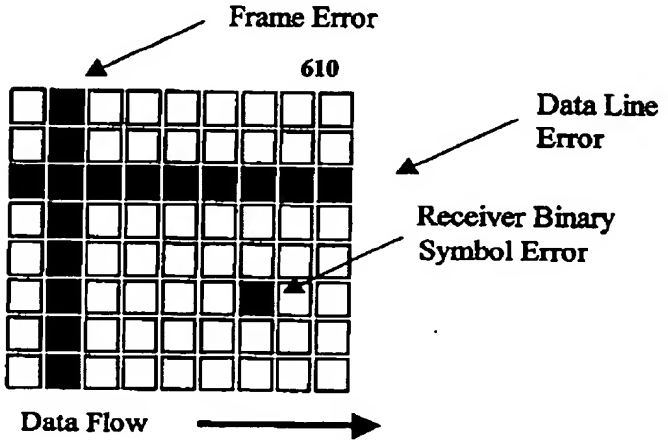


FIG 6B

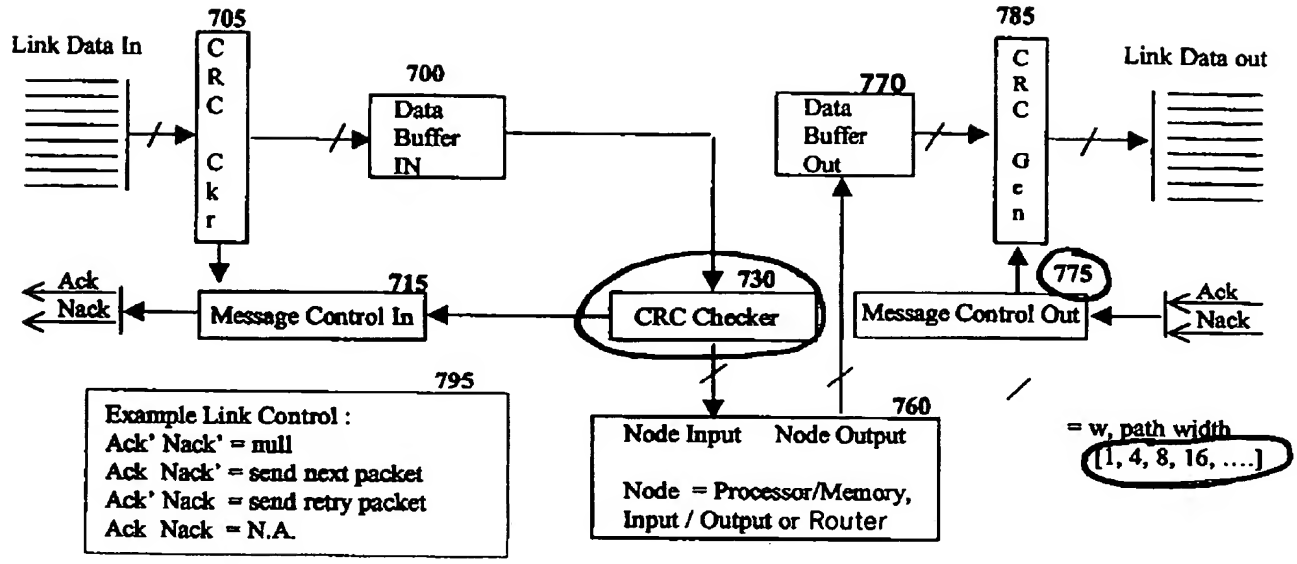

Link Data In
705
CRC Ckr
700
Data Buffer IN
770
Data Buffer Out
785
CRC Gen
Link Data out
Ack
Nack
715
Message Control In
730
CRC Checker
775
Message Control Out
Ack
Nack
795
Example Link Control :
Ack' Nack' = null
Ack Nack' = send next packet
Ack' Nack = send retry packet
Ack Nack = N.A.
760
Node Input Node Output
Node = Processor/Memory,
Input / Output or Router
= w, path width
[1, 4, 8, 16, ...]

FIG 7

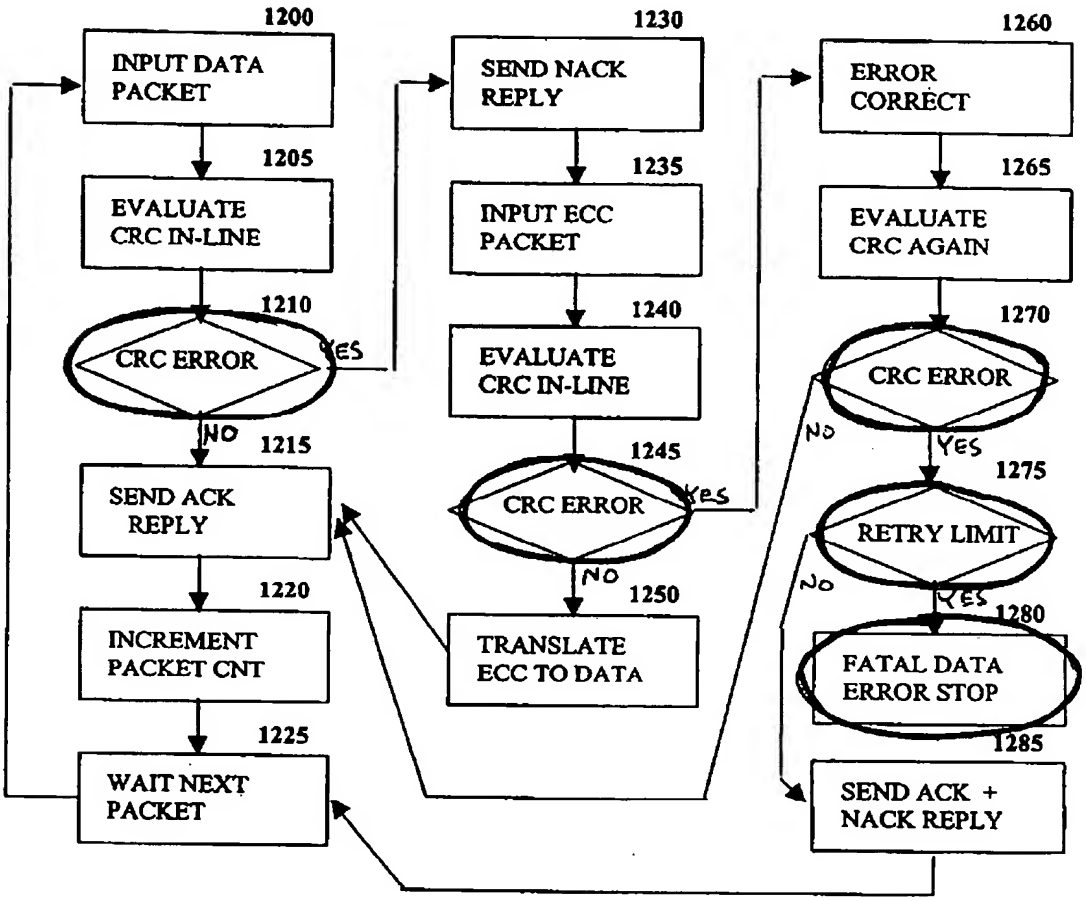

1200
INPUT DATA PACKET
1205
EVALUATE CRC IN-LINE
1210
CRC ERROR
YES
NO
1215
SEND ACK REPLY
1220
INCREMENT PACKET CNT
1225
WAIT NEXT PACKET
1230
SEND NACK REPLY
1235
INPUT ECC PACKET
1240
EVALUATE CRC IN-LINE
1245
CRC ERROR
Yes
NO
1250
TRANSLATE ECC TO DATA
1260
ERROR CORRECT
1265
EVALUATE CRC AGAIN
1270
CRC ERROR
NO
Yes
1275
RETRY LIMIT
NO
Yes
1280
FATAL DATA ERROR STOP
1285
SEND ACK + NACK REPLY

FIG 12

[E] 1301								[D] 1300							
c6uc2u	u30	u26	u22	u18	u14	u10	u06	u02	c4sc0s	s28	s24	s20	s16	s12	s08	s04	s00
c6vc2v	v30	v26	v22	v18	v14	v10	v06	v02	c4tc0t	t28	t24	t20	t16	t12	t08	t04	t00
c7uc3u	u31	u27	u23	u19	u15	u11	u07	u03	c5sc1s	s29	s25	s21	s17	s13	s09	s05	s01
c7vc3v	v31	v27	v23	v19	v15	v11	v07	v03	c5tc1t	t29	t25	t21	t17	t13	t09	t05	t01
c4uc0u	u28	u24	u20	u16	u12	u08	u04	u00	c6sc2s	s30	s26	s22	s18	s14	s10	s06	s02
c4vc0v	v28	v24	v20	v16	v12	v08	v04	v00	c6tc2t	t30	t26	t22	t18	t14	t10	t06	t02
c5uc1u	u29	u25	u21	u17	u13	u09	u05	u01	c7sc3s	s31	s27	s23	s19	s15	s11	s07	s03
c5vc1v	v29	v25	v21	v17	v13	v09	v05	v01	c7tc3t	t31	t27	t23	t19	t15	t11	t07	t03

Data Flow >>> <<< NACK <<< ACK

FIG 13

[E] 1401								[D] 1400							
c6uc2u	u30	u26	u22	u18	u14	u10	u06	u02	c4sc0s	s28	s24	s20	s16	s12	s08	s04	~~s00~~
c6vc2v	v30	v26	v22	v18	v14	v10	v06	v02	c4tc0t	t28	t24	t20	t16	t12	t08	t04	t00
c7uc3u	u31	u27	u23	u19	u15	u11	u07	u03	c5sc1s	s29	s25	s21	s17	s13	s09	s05	s01
c7vc3v	v31	v27	v23	v19	v15	v11	v07	v03	c5tc1t	t29	t25	t21	t17	t13	t09	t05	t01
c4uc0u	u28	u24	u20	u16	u12	u08	u04	~~u00~~	c6sc2s	s30	s26	s22	s18	s14	s10	s06	s02
c4vc0v	v28	v24	v20	v16	v12	v08	v04	v00	c6tc2t	t30	t26	t22	t18	t14	t10	t06	t02
c5uc1u	u29	u25	u21	u17	u13	u09	u05	u01	c7sc3s	s31	s27	s23	s19	s15	s11	s07	s03
c5vc1v	v29	v25	v21	v17	v13	v09	v05	v01	c7tc3t	t31	t27	t23	t19	t15	t11	t07	t03

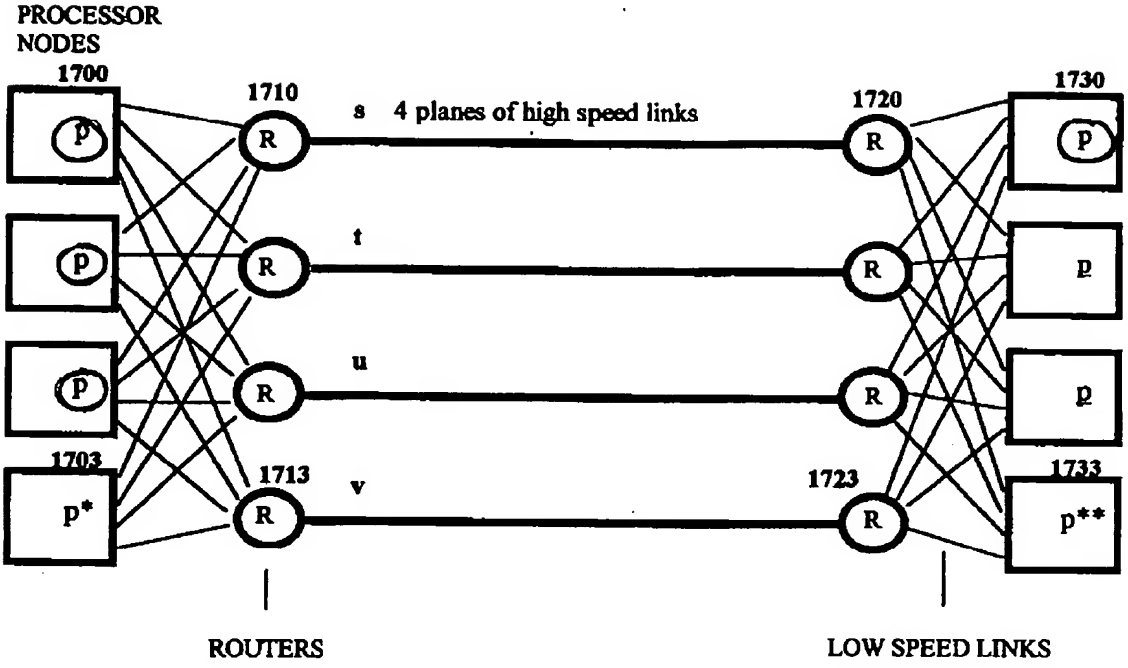
Data Flow >>> <<< NACK <<< ACK

FIG 14

Begin with Byte 00
Transmitted
s00t00 = 18h (data = ts = 81h) **u00v00 = 77h (ECC = vu = 77h)**
Received
s00t00 = 1Ah (data = ts = A1h) **u00v00 = 75h (ECC = vu = 57h)**
So correction proceeds exactly as before in Figure 8 for byte 00.
All 32 bytes are assembled and corrected then verified via the CRC checkcode comparison.

	ECC	Data
Data byte 00 input in error is		1 0 1 0 0 0 0 1 = A1 hex.
The ECC for A1 is F8	1 1 1 1 1 0 0 0 = F8 hex.	
ECC byte 00 input in error is	0 1 0 1 0 1 1 1 = 57 hex.	
The ECC syndrome	1 0 1 0 1 1 1 1 = AF hex.	
E.P. from Table 1 = d5 & e5	0 0 1 0 0 0 0 0 = e5	and 0 0 1 0 0 0 0 0 = d5
After corrections data = 81 hex.	0 1 1 1 0 1 1 1 = 77 hex.	and 1 0 0 0 0 0 0 1 = 81 hex.

FIG 14A


PROCESSOR NODES
1700
1710
s
4 planes of high speed links
1720
1730
t
u
1703
1713
v
1723
1733
p*
p**
ROUTERS
LOW SPEED LINKS

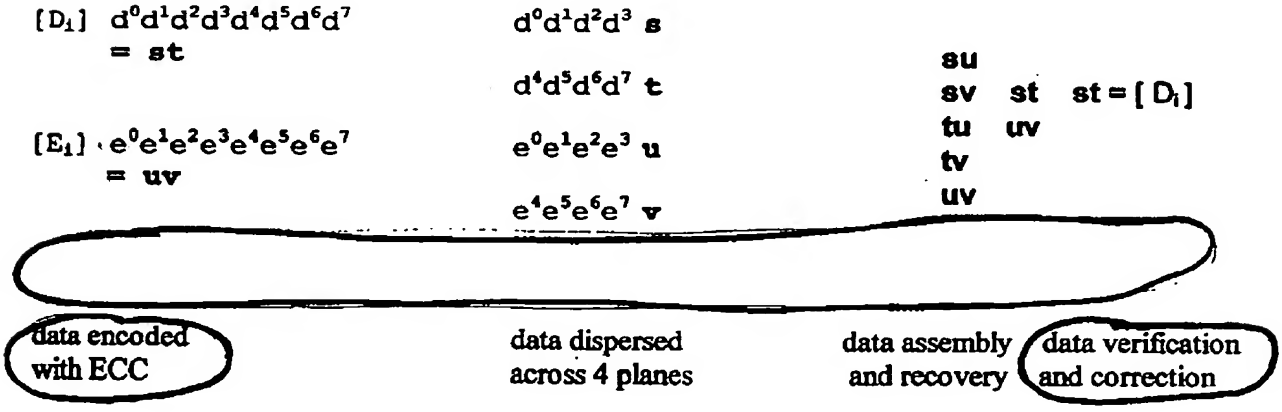

[D1] d0d1d2d3d4d5d6d7 = st
[E1] e0e1e2e3e4e5e6e7 = uv
d0d1d2d3 s
d4d5d6d7 t
e0e1e2e3 u
e4e5e6e7 v
su
sv st st = [D1]
tu uv
tv
uv
data encoded with ECC
data dispersed across 4 planes
data assembly and recovery
data verification and correction

FIG 17